# Total Dose Test Report for Toshiba 128M NOR Flash Nonvolatile Memory

Test Date: 8/22/2006 Report Date: 8/29/2006

## I. Introduction

The purpose of this test was to determine the susceptibility to total ionizing radiation dose (TID) of the Toshiba 128M NOR flash nonvolatile memory (part number TC58FVM7B2ATG-65-ND, Lot Date Code 0539). This test was supported by the NASA Electronics Parts and Packaging (NEPP) Program.

## II. Devices Tested

The Toshiba NOR Flash Memory is a non-volatile memory that uses a floating gate NOR cell. It also provides a standard interface for pin and function drop-in compatibility. We believe these parts were burned-in before leaving the factory, so it is not possible to do a controlled experiment to look at burn-in effects. In any case, there is no plan to do our own burn-in. Detailed device information is provided in Table I. In this case, eight samples were irradiated, and there was also one unirradiated control device. The parts have a nominal 3.3 V power supply, plus an internal charge pump to generate higher voltages for writing and erasing.

**Table I**. Device information

| | |
|---|---|
| **Full Part Number** | TC58FVM7B2ATG-65-ND |
| **Manufacturer:** | Toshiba |
| **Lot Date Code (LDC):** | 0539 |
| **Quantity Tested:** | 9 |
| **Serial Numbers of Control Sample:** | 9 |
| **Serial Numbers of Radiation Samples:** | 1,2, 3, 4, 5, 6,7,8 |
| **Part Function:** | NOR Flash Memory |
| **Part Technology:** | CMOS |
| **Case Markings:** | Toshiba F9040<br>Japan 0539KAD<br>TC58FVM7B2ATG65 |
| **Package Style:** | 56 pin TSOP |
| **Test Equipment:** | Power Supply (+3.3V)<br>Digital test board.<br>Multimeters |
| **Test Engineer:** | M. Friendlich |
| **Dose Levels (krad (Si)):** | 10, 20, 30, 50, 75, and 100krads(Si) continuing in 50krads (Si) steps until functional failure. |
| **Target dose rate (rad (Si)/min):** | 1200-1800 |

## III. Test Facility

Testing was at the Co-60 facility at GSFC, which is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry is performed, using air ionization probes. Testing is done in a step/stress manner, using a standard Pb/Al filter box. Dose rate typically varies slightly from one exposure to the next, up to 30 rads/s. Most exposures are near the maximum dose rate, as required by MIL-STD Test Method 1019.6. Time intervals for testing between exposures are also within the limits stated in 1019.6 (one hour after exposure to start electrical characterization, two hours to begin the next exposure). Parts were under DC bias during exposures, but not actively exercised.

## IV. Test Procedure

The test devices were programmed with a checkerboard pattern (AA) during exposures, and biased at 3.6 V (3.3 V nominal power supply, plus 10%), but the devices were not actively exercised during exposures. Four parts were read (only) between exposures, to look for problems related to the integrity of the individual bits. The other four parts were exercised between exposures—read, erased, and written into four different patterns. The patterns were checkerboard (AA), checkerboard complement (55), all ones, and all zeroes. In each of these tests, the entire memory is read, or erased, or programmed in one operation, with the commands entered manually. There is also a dynamic test mode, where each block is read, erased, and programmed, then the next block, and so on until the entire memory is completed. A block diagram of the test apparatus is shown in Fig. 1.

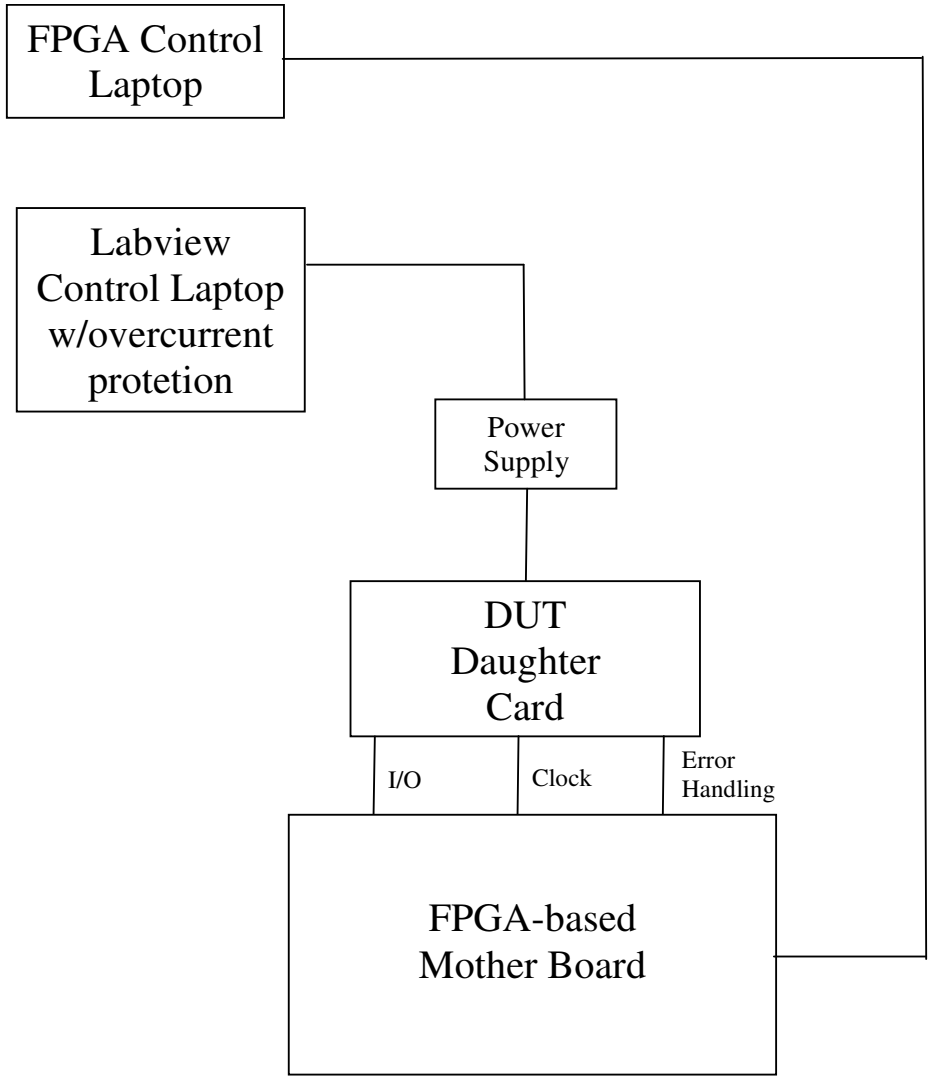


Fig. 1. Block diagram of the flash memory test apparatus.

## V. Results

DUTs 1-4 were tested in read-only mode, while DUTs 5-8 were exercised in all the test patterns and the dynamic mode, as described above. Even at the 10 krad ($SiO_2$) exposure level, the erase function had failed on DUTs 5, 7, and 8. DUT 6 erased successfully, but could not be written. DUTs 1-4, in read-only mode, had no errors. At the 20 krad ($SiO_2$) exposure level, DUTs 1-4 still had no errors. At the 30 krad ($SiO_2$) exposure level, errors were observed in the read-only devices, although the error count varied slightly on successive reads. DUT 1 had 0-3 errors, and DUT 3 had 3-5 errors. DUTs 2 and 4 still had no errors. Although the original plan had been to do the next exposure to 50 krad ($SiO_2$), the decision was made to stop at 40 krad, because complete failure seemed to be near. At the 40 krad ($SiO_2$) exposure level, all the devices had significant numbers of errors. DUTs 2 and 4, which had no errors before, had 162 and 500 errors, respectively. DUTs 1 and 3, which previously had single digit error counts, had 14300 and 4900 errors respectively. After errors were detected, we tried to reset the bits, but the erase and write circuits had both failed.

## VI. Recommendations

In general, devices are categorized based on heavy ion test data into one of the four following categories:

Category 1: Recommended for usage in all NASA/GSFC spaceflight applications.
Category 2: Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
Category 3: Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.
Category 4: Not recommended for usage in any NASA/GSFC spaceflight applications.
Research Test Vehicle: Please contact the P.I. before utilizing this device for spaceflight applications

The Toshiba TC58FVM7B2ATG-65-ND NOR flash has not yet been characterized for Single Event Effects (SEE). It is expected to be Category 4, when more complete data is available.